AMENDMENTS TO THE SPECIFICATION

Please add the following new heading and paragraph numbered as [0000] before paragraph [0001] beginning on page 1:

CROSS-REFERENCE TO RELATED APPLICATIONS

[0000] This application is a continuation of and claims priority to copending and commonly assigned United States patent application serial number 10/171,915 entitled "Dual Input, Hot Swappable Dual Redundant, Enhanced N+1 AC to DC Power System," filed June 14, 2002, United States patent application serial number 09/940,973 entitled, "Dual Input, Hot Swappable Dual Redundant, Enhanced N+1 AC to DC Power System," filed August 28, 2001, and United States patent number 6,356,470 entitled, "Dual Input, Hot Swappable Dual Redundant, Enhanced N+1 AC to DC Power System," issued March 12, 2002, the disclosures of which are hereby incorporated herein by reference.

Please substitute the following marked-up paragraphs for the paragraphs now appearing in the currently filed specification:

Please amend paragraph [0002] as follows:

[0002] Large, multi-processor computer systems are business enterprise servers for use by large corporations with high speed computer needs, e.g. automotive companies, large accounting firms, Internet companies, etc. Enterprise servers take large amounts of AC current from the site power, typically on the order of 10-20 kilowatts of power. Therefore, 3-phase power is usually used to power these systems. One of the major ~~requirement~~ requirements for enterprise servers is what is called high availability. The meaning here is that there is the desire that there are no external events that force the machine to crash. One common event that leads to a system crash is loss of the system power. This may occur as a result of a commercial power producer problem or it may originate with loss of a system power component. Note that with ~~three-phase~~ three-phase power, the problem can be from the loss of the entire 3-phase grid, or loss of one of the three legs.

Please amend paragraph [0006] as follows:

[0006] Each BPS is split into two halves, with each ~~halve~~ half being run by a separate power grid. This means that if one of the power grids goes down, the other grid fills the power. Thus, because there are no switching times or latencies, the inventive power supply system keeps running. When both power grids are present, each power supply ~~halve~~ half in a BPS load shares 50/50. To make this possible, it ~~was~~ is necessary to be able to accommodate two input power grids of basically any voltage between 176 and 284 VAC. The phase relationship of these voltages is unimportant.

Please amend paragraph [0009] as follows:

[0009] It is another a technical advantage of the present invention to be able to have a ~~two-way~~ two-way redundant power supply. One is AC input power redundancy, via two PDCAs. The other is DC power redundancy, via N+1 BPSs.

Please amend paragraph [0017] as follows:

[0017] FIGURE 1 depicts a functional block diagram for the preferred embodiment of the inventive power supply system 100. In this system, six bulk power supplies (BPSs) 101 are used. Note that this number is for illustration only, as more or fewer BPSs could be used, as long as there are N+1 present. Each BPS receives power via a connecting backplane or chassis 102. The chassis 102 is connected to two power grids, 103, 105 via power distribution control assemblies (PDCAs) 104, 106. Note that each PDCA 104, 106 is feeding each BPS 101. The BPSs 101 form a 48-volt output and a 5-volt DC ~~outputs,~~ output, which are provided back to the chassis 102 for distribution to other components of the system, e.g. the main computer processor boards, via buses 107, 108. Note that the voltage levels and the number of levels ~~is~~ are by way of example only, as system requirements may have different voltage levels as well as a different number of levels.

Please amend paragraph [0018] as follows:

[0018] The PDCAs 104, 106 can be field-configured to accept 3-phase delta, 3-phase wye, or single phase as the power source, depending on the grid 103, 105 being used. The phase legs of the three phase inputs are arranged such that legs, L1, L2, and L3, each feeds two BPS slots. Each BPS receives an input from each PDCA. Thus, a power loss from one of the PDCAs would only disable one-half of each BPS. Each BPS is connected to a

power monitor ~~(301 of FIGURE 3)~~ (301 of FIGURE 3) via control signals 106. These signals allow for each BPS to be powered up/down, as ~~wells~~ well as send and receive status information. 5VHK J2 108 is a +5 volt DC output used for end-system housekeeping (HK).

Please amend paragraph [0019] as follows:

[0019] FIGURE 2 depicts the functional block diagram for the preferred embodiment of ~~a~~ BPS 101. The BPS includes line filter blocks 201, 202 and rectifier blocks 213, 216 that receive the two AC inputs. The EMI filter portion suppresses harmonic signals from reflecting back into the AC input lines. The rectifier blocks rectify the AC input power into DC power. The filtered DC output is provided to PFC blocks 214, 217 which ensure a power factor of greater than about ~~.98.~~ 0.98. Their outputs are provided to converters ~~203/204~~ 203, 204 for the +48 voltage level and 205 for the +5 ~~volt~~ voltage level. The outputs of the converters are sent to isolation diodes/output filters 206. The isolation diodes are necessary for hot swapping and the output filter elements are capacitors. The BPS uses fans 207 to cool the BPS. Bias supplies 215, 219 supply power to the fans 207 and the control logic 209. Output terminals 211 ~~receives~~ receive the ~~48-volt~~ 48-volt output from the filter 206, which is then delivered back to the chassis 102. Output connector 212 receives the ~~5 volt~~ 5-volt output from the filter 206, which is then delivered back to the chassis 102. Load share controller 208 operates to control load sharing of the +5VHK. Control logic 209 controls the other elements of the BPS, as well as sends/receives status information to/from the power monitor 301 via connector 210. Substantially instantaneous switching without using a switch is accomplished by having two converter chains (i.e. 201, 213, 214, 203; and 202, 216, 217, 204). If one chain should drop off, the other chain sees a higher load, and then increases its power output. In other words, each chain is capable of fully satisfying the load for the BPS.

Please amend paragraph [0020] as follows:

[0020] FIGURE 3 depicts the functional block diagram for the preferred embodiment of how ~~a~~ BPS 101 connects ~~with~~ to PDCAs 104, 106. The power monitor 301 receives AC status information 302, BPS status information 303, as ~~wells~~ well as send commands to the BPSs via 303. The power monitor is a consumer of the ~~5-volt~~ 5-volt power supply from 108. Note that the monitor 301 is not part of the BPS or power supply system,

but rather is part of an end-product computer system. In the depicted example, the PDCAs are provided with 3 phase AC power, which they convert into three single phase pairs. PDCA 104 (shown for delta connection) provides input pairs A1, A2, A3, and ground to the BPSs. PDCA 106 provides input pairs B1, B2, B3, and ground to the BPSs. The As and Bs are two wire pairs of AC power. Each input signal feeds two BPSs, and if there are more/fewer BPSs, then each input signal would feed more/fewer BPSs. In the depicted example, the A1 pair goes to BPS slots 0 and 1, the A2 pair goes to BPS slots 2 and 3, and the A3 pair goes to BPS slots 4 and 5. Similarly, the B1 pair goes to BPS slots 0 and 1, the B2 pair goes to BPS slots 2 and 3, and the B3 pair goes to BPS slots 4 and 5. Note that this is for illustration purposes only, as different pairs of As and Bs could feed different BPS slots. Each PDCA contains wiring to convert the three phase input into three single phase outputs, where the legs, L1, L2, L3 of the three phase input are wired to the outputs A1, A2, A3, B1, B2, and B3 as follows:

Please amend paragraph [0023] as follows:

[0023] Although the invention has been described in terms of ~~three phase~~ three-phase power grids, ~~103, 104. These~~ 103,104, these grids could either or both be large single phase grids. In that case, the wiring in the PDCA would be a ~~6-way~~ 6-way split of the input power grid, with one line to each slot.